



Intermediate ASIC Design Engineer

GEO Semiconductor is staffing a team for its next generation warp chip which will be a complete SOC targeted for many high-volume consumer applications using state-of-the art design and process technologies. We are looking for highly motivated individuals who are interested in contributing in all phases of the product development. As a startup, this provides a great opportunity to expand one's experience and knowledge base to encompass all aspects of ASIC design.

As a critical member of the ASIC team, your responsibilities will include RTL design, synthesis, timing closure, low-power design, block-level documentation & verification, gate sims and lab validation.

Qualifications:

- 5 years ASIC design or verification experience in multimillion gate chips.
- Programming experience in Verilog, C are required. TCL/PERL are assets.
- Video processing, and DSP knowledge is desired.
- Strong communication and interpersonal skills required to work in a team.
- Tapeout experience: SDF gate sims, ECOs and timing closure.
- Experience in high-volume production chips, and low-power design techniques is a plus.
- Bachelor's degree in Electrical Engineering required. MS degree an asset.